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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,088	08/15/2001	Eugene W. Lee	3981-6	2875

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EXAMINER	
DAVIS, ZACHARY A	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,088	LEE ET AL.	
	Examiner	Art Unit	
	Zachary A. Davis	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. An amendment was received on 08 July 2005. Claims 19-24 have been amended. New Claims 25-30 have been added. Claims 1-18 have been canceled. Claims 19-30 are currently pending in the present application.

Response to Arguments

2. Applicant's arguments with respect to claims 19-30 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. The objections to the drawings for failing to comply with 37 CFR 1.84(p)(5) are withdrawn in light of the amendments to the specification.

4. The objection to the drawings regarding typographical and other errors is **NOT** withdrawn. Applicant asserts that Applicant was unable to locate the misspelled label "Scambler Polynomial" in Figure 4, and Applicant further asserts that the correct flow directions between elements 104 and 112 and between elements 116 and 108 are shown in Figure 8. Although the Examiner notes that these errors are not present in the drawings originally filed with the application on 15 August 2001, the errors are indeed present in the formal drawings received 02 January 2002 (as cited in the previous Office

action). These were the drawings published in US Patent Application Publication 2003/0044005, which has been cited for Applicant's convenience.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 23, 24, and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites the limitation "the first array of de-scrambled output bits" in line 3. There is insufficient antecedent basis for this limitation in the claims, although it appears that this is intended to refer to the "first array of de-scrambled packet bits". Claim 24 is rejected due to its dependence on rejected Claim 23.

Claim 30 recites the limitation "the first de-scrambled output bits". There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 19-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al, US Patent 6862701, in view of Suemura, US Patent Application Publication 2001/0008001.

In reference to Claim 19, Walker discloses a device including an ingress circuit for processing packets received over a network (Figure 4, receiver 122; column 9, lines 37-49), an egress circuit for processing packets for sending over the network (Figure 4, transmitter 120; column 9, lines 44-49), and a scrambler circuit that scrambles a parallel array of input bits into an array of scrambled output bits (column 15, lines 39-42). However, although Walker discloses inputs and outputs for transferring packets between the ingress and egress circuits (Figure 4, bus 18 and 19; see also column 1, lines 38-44), Walker does not explicitly disclose a switch fabric, nor that the scrambler scrambles packet bits received from the ingress circuit.

Suemura discloses a device including an ingress circuit for processing packets received over a network (Figure 1, input interfaces 2.0-2.3; paragraph 0064), an egress circuit configured to process packets for sending over the network (Figure 1, output interfaces 4.0-4.3; paragraph 0065), a reconfigurable switch fabric for transferring scrambled data between a plurality of ports (Figure 1, optical switch 3; paragraph 0065), and a first scrambler circuit that scrambles a first parallel array of packet bits received from the ingress circuit into a first array of scrambled output bits for sending across the switch fabric to the egress circuit (Figure 3, scrambler 31; paragraphs 0068, 0071-0076). Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify the device of Walker to include a switch fabric and scrambling of data before sending to the switch fabric, in order to allow synchronization of scramblers when scrambling is applied to an internal signal of a switching system (see Suemura, paragraph 0027).

In reference to Claim 20, Walker further discloses a new seed register for storing the first array of scrambled output bits and supplying the first array of scrambled output bits to apply to a second array of bits (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254). Suemura also discloses a new seed register for storing an array of scrambled bits to apply to a second array of bits (see paragraph 0073; see also paragraphs 0091-0095).

In reference to Claim 21, Walker further discloses a second scrambler circuit in the egress circuit for scrambling the packets before sending those packets over the network (Figure 4, Scrambler 133; column 9, lines 45-54), and a second new seed register (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254).

In reference to Claim 22, Suemura further discloses a first de-scrambler coupled to the egress circuit that receives the first array of scrambled output bits and de-scrambles the first array of scrambled output bits into a first array of descrambled bits ().

In reference to Claim 23, Walker further discloses a new seed register for storing the first array of de-scrambled bits and supplying the first array of de-scrambled bits to apply to a second array of scrambled bits (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254; see column 17, lines 36-42, noting that a de-scrambler can be made by rearranging the scrambler). Suemura also discloses a new seed register

storing an array of de-scrambled bits to apply to a second array of bits (see paragraph 0073; see also paragraphs 0091-0095).

In reference to Claim 24, Walker further discloses a second de-scrambler circuit in the ingress circuit for descrambling arrays of scrambled bits received from the network (Figure 4, De-Scrambler 138; column 9, lines 45-60), and a second de-scrambler new seed register (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254; see column 17, lines 36-42, noting that a de-scrambler can be made by rearranging the scrambler).

In reference to Claim 25, Walker discloses a method including receiving packet data from a network (Figure 4, receiver 122; column 9, lines 37-49), scrambling a parallel array of bits from the packet data into an array of first scrambled output bits (column 15, lines 39-42), and descrambling the first scrambled output bits (see column 17, lines 36-42). However, although Walker discloses inputs and outputs for transferring packets between the ingress and egress circuits (Figure 4, bus 18 and 19; see also column 1, lines 38-44), Walker does not explicitly disclose transferring scrambled bits through a switch fabric, nor does Walker explicitly disclose descrambling scrambled bits after transferring the scrambled bits through a switch fabric.

Suemura discloses a method including receiving packet data from a network (Figure 1, input interfaces 2.0-2.3; paragraph 0064), scrambling a first parallel array of bits from the packet data into an array of first scrambled output bits (Figure 3, scrambler 31; paragraphs 0068, 0071-0076), transferring the first scrambled output bits through a

reconfigurable switch fabric (Figure 1, optical switch 3; paragraph 0065), and descrambling the first scrambled output bits after transferring the first scrambled output bits through the switch fabric (Figure 6, descrambler 45; paragraphs 0079, 0084-0090). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Walker to include a transferring scrambled bits through a switch fabric descrambling the scrambled bits after transfer through the switch fabric, in order to allow synchronization of scramblers when scrambling is applied to an internal signal of a switching system (see Suemura, paragraph 0027).

In reference to Claim 26, Walker further discloses storing the first scrambled output bits as new seed values for applying scramble polynomials to a second array of bits (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254). Suemura also storing new seed values (see paragraph 0073; see also paragraphs 0091-0095)

In reference to Claim 27, Walker further discloses selecting the new seed values according to a polynomial value, a bit length, and a bit position (column 15, lines 39-42; column 16, lines 12-50; see Figure 7). Suemura also discloses selecting new seed values according to a polynomial value, bit length, and bit position (paragraph 0073).

In reference to Claim 28, Walker further discloses that a 1+X(39)+X(58) scramble polynomial is applied to each bit (column 15, lines 39-42).

In reference to Claim 29, Walker further discloses that de-scrambling includes receiving first scrambled bits, storing an array of previously de-scrambled output bits, and applying the array of previously de-scrambled bits during descrambling of the scrambled bits (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254;

see column 17, lines 36-42, noting that a de-scrambler can be made by rearranging the scrambler). Suemura also discloses that de-scrambling includes receiving scrambled bits, storing previously de-scrambled bits, and applying the previously de-scrambled bits (paragraph 0085; see also paragraphs 0091-0095).

In reference to Claim 30, Walker further discloses storing de-scrambled output bits as new seed values for applying to a next group of scrambled output bits (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254; see column 17, lines 36-42, noting that a de-scrambler can be made by rearranging the scrambler). Suemura also discloses storing de-scrambled bits to apply to a next group of scrambled bits (paragraph 0085; see also paragraphs 0091-0095).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary A. Davis whose telephone number is (571) 272-3870. The examiner can normally be reached on weekdays 8:30-6:00, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ZAD
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